

### R E M A R K S

Careful review and examination of the subject application are noted and appreciated. Applicant's representative thanks Examiner Cho for the indication of allowable matter.

### IN THE DRAWINGS

The objection to the drawings has been obviated by appropriate amendment and should be withdrawn. Applicant herewith submits replacement drawing sheets including (i) amendments to FIGS. 1 and 2 as approved by the Examiner (see page 2, section no. 2 of the Office Action) and (ii) amendment to FIG. 6 to illustrate an AND plane as required by the Examiner (see page 3, section no. 3 of the Office Action). Support for the amendment to FIG. 6 can be found in the claims as originally filed, for example, claim 14, and in the specification as originally filed, for example, on page 1, lines 10-20, on page 2, lines 8-16, on page 7, lines 7-8 and on page 10, lines 15-18.

Specifically, the specification states:

**"A programmable logic device (PLD) provides an economical and efficient means for implementing predetermined Boolean logic functions in an integrated circuit. Such a device consists of, generally, an AND plane configured to generate predetermined product terms in response to a plurality of inputs, a group of fixed/programmable OR gates configured to generate a plurality of sum-of-**

product(SOP) terms in response to the product terms, and a number of logic elements (i.e., macrocells) configured to generate a desired output in response to the sum-of-products terms. The sum-of-products terms can also be generated using programmable NOR-NOR logic." (page 1, lines 10-20 of the specification, emphasis added).

The specification further states that "[t]he plurality of inputs [to the AND plane] are presented by product term input circuits" (page 2, lines 11-12 of the specification).

Since the specification states that the circuit 200 illustrated in FIG. 6 of the specification may be implemented as a product term input circuit of a programmable logic device (see page 10, lines 15-18 of the specification) and it is known in the art that product term input circuits present inputs to an AND plane in a programmable logic device, it follows that the specification provides support for the addition to FIG. 6 of the block labeled AND plane with an input connected to the circuit 200. As such, no new matter has been introduced.

#### IN THE SPECIFICATION

The specification has been amended for consistency. Support for the amendment to the specification can be found in the claims as originally filed, for example, claim 14, and in the specification as originally filed, for example, on page 1, lines

10-20, on page 2, lines 8-16 and on page 10, lines 15-18. As such, no new matter has been introduced.

**CLAIM REJECTIONS UNDER 35 U.S.C. §102**

The rejection of claims 6 and 13-15 under 35 U.S.C. §102(b) as being anticipated by Turner et al. (U.S. Patent No. 4,879,688, hereinafter Turner) has been obviated by appropriate amendment and should be withdrawn.

Subject matter believed to be similar to the allowable matter of claim 16 has been incorporated into claim 6. Claims 7-17 depend, either directly or indirectly, from claim 6, which is now believed to be allowable. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

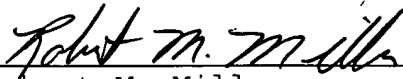
The Examiner is respectfully invited to call the Applicant's representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office

Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.

  
Robert M. Miller  
Registration No. 42,892  
24025 Greater Mack, Suite 200  
St. Clair Shores, MI 48080  
(586) 498-0670

Dated: April 13, 2004

Docket No.: 0325.00353